"TouchScreen" project

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Updated RiscList V0.4
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This documentation contains the updated RiscList
of the project "TouchScreen TI6"

V0.1	2006-10-20	Initial Release
V0.2	2006-10-23	estimation of man-power
V0.3	2006-10-30	corrections after meeting
V0.4	2006-11-03	additional functionality => new riscs
V0.5	2006-11-13	new riscs

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1 Staff in the laboratory

The restricted laboratory opening times, limits the access to the laboratory staff. This leads to restricted possibilities of developing the touchscreen. (Request for better opening times)

2 Given materials containing errors

The VHDL of the "Einfachstrechner" in the FPGA and the given JAVA-assembler-program could contain errors that are very difficult to find and fix. Not all sources could be checked by the team at the moment, cause of the huge amount of source code. The "Einfachstrechner" represents a part of the product which is essential, we hope there are no unknown bugs inside.

3 The board

On the backside of the board are a lot of cables soldered to the board. If one cable gets lost, this could lead in a delay.

It is not clear if the touch panel interface is seriously tested, i.e. if it really works! (manual test!)

4 Loss of developed data

If we would loose already programmed source code, we would have to do it twice. But that represents a very low risc because we are using SVN[1] and all data are stored on several PCs. (Request to software lab?)

5 Estimation of needed man-power

It is hard to estimate the needed man-power for all our defined visions. We should be very careful which parts (debugger, RAM loader, feature rich Editor) we want to realise.

6 ARM write routine

During the transfer of the HEX-Machine-Code from E.R.D.E to the ARM the ARM has to buffer the received data and transfer it to the ER.

[1] Subversion (SVN) ist an Open-Source-Software versionmanagement

The synchronisation of these two transfers could be a problem. We do not know how difficult the transfer from the ARM to the ER is, cause it seems that we have to modify the adressdecoder. We do not know if the buffer of the ARM is big enough.

7 ER ROM writeable by ARM

The ROM of the ER has to be realized as a RAM to be writeable by the ARM.

We do not know yet if the FPGA is big enough for the additional functionality. But seems to be big enough.

8 FPGA malfunction

The FPGA could get damaged by a mistake in the VHDL-model. For example two outputs on the same signal (one high & other low).